QIE8

Tom Zimmerman
July 22, 2001

The QIE8 is the latest addition to the "family" of QIE devices. It is the first of a new generation of parts which contain major design changes and improvements over the older versions of QIE. QIE8 is produced in the AMS 0.8u BiCMOS process, a "true" BiCMOS process (previous QIE's were produced in the pseudo-BiCMOS 2u ORBIT process).

QIE8 integrates input charge in 25 nS buckets over a large dynamic range and digitizes the result with nearly constant resolution over the entire range. It accomplishes this by integrating the charge on four ranges with different sensitivities, and selecting one range based on the signal magnitude. The integrator output is fed to a custom on-chip pseudo-logarithmic FADC which digitizes the result. The bit size of the ADC changes in piecewise linear fashion over its range to tend to keep the (bit size)/(signal magnitude) ratio constant. The QIE8 outputs are then purely digital, a 2-bit range number and a 5-bit FADC output.

QIE8 has two independent input amplifiers, one inverting and one non-inverting so that it can accept either polarity input signal. The non-inverting input is meant to accept a fast negative current PMT signal driven down a cable of significant length. It therefore has an impedance which is nearly constant over the entire range, in order to properly terminate a cable. The input impedance is selectable between two values, 50 and 93 ohms. The amplifier gain is approximately one, resulting in a nominal low end sensitivity of 2.6 fC/ bit. The maximum charge accepted per bucket is nominally 26 pC, yielding a 10,000:1 dynamic range, or at least 13 bits. The non-inverting amplifier has a fast response to allow complete integration of a fast PMT pulse in one 25 nS bucket.

The inverting amplifier is meant to accept positive current input pulses from HPD's. Since HPD signal levels are low, the amplifier has a current gain of –2.6, resulting in a low end sensitivity of 1 fC/bit. The maximum input charge per bucket is then approximately 10 pC. Since HPD pulses are slower (typically over several buckets), the inverting amplifier response is slower than the non-inverting amplifier, in order to limit noise. Also, its input impedance is low (30 ohms or less) but not constant over the full range, since this input is intended to be driven with a relatively short cable.

The user must select which input amplifier will be used by powering only the one desired, and grounding the VDD pin of the amplifier which will not be used.

The QIE8 die has 64 pads which must be bonded. It is intended to be packaged in a 64 pin package. However, the fact that the number of chip pads and package pins is identical is actually quite coincidental. This is due to the fact that the chip is bonded in a non-standard fashion – each bondpad does not necessarily go to a package pin. The metal die pad inside the package serves as "system ground," and all of the chip ground pads are bonded directly down to the die pad inside the package. The die pad is then bonded out to a number of package ground pins in various locations.

The following pin naming conventions are observed: Inputs and control pins which are associated with the non-inverting input are prefaced with **NI_**. Inputs and control pins which are associated with the inverting input are prefaced with **I_**.

Every input pin is surrounded on both sides by ground pins. Each input that is routed to the QIE8 on a PC board must be routed on an inner layer and fully enclosed by ground planes and traces. The ground planes should come at least up to the input side of the package, where they must connect directly to all 8 ground pins on that side of the package. No other "analog ground plane" is needed on the PC board. Supporting digital circuitry on the PC board should be placed nearest the QIE8 output edge, completely away from the input edge. There should be a "digital ground plane" for all digital circuitry on the PC board. This plane should extend under the QIE8 digital output traces (but should not extend under the QIE8) and be connected to the QIE8 ground at ONE place only, the DGND1,2 pins.

Analog and digital power pins (**AVDD** and **DVDD**) can be driven by a single supply regulator (5.0V min., 5.5V max.). However, the pins should not be tied to a "power plane." Separate traces which are tied together close to the 5V regulator should supply these pins. The supply regulator ground should connect to the PC board digital ground plane.

The non-inverting and inverting input amplifier sections each have their own analog supply pins (**NI_AVDD** and **I_AVDD**). Only one amplifier is intended to be used at a time (although theoretically both could be used simultaneously). The unused amplifier should have its AVDD pin tied to ground.

The **AGND** pins on the left edge do not necessarily need to be connected to "ground plane." They are provided to offer easy routing of **AVDD** and **NI_CLAMP** bypass capacitors (**AGND** pins connect the caps to the internal die pad ground).

A digital supply bypass capacitor is required, but must NOT be placed to any ground plane. It should simply be connected from the **DVDD** pins to the **DGBYP** pin.

The following list is a description of the pins of the packaged QIE8. The package pins are numbered from 1 to 64, starting in the upper left corner and proceeding counterclockwise.

1. **CAPID(1)**. Cap ID output MSB. (Cap ID is a 2 bit number representing which of the four pipelined integrating capacitors is being read out). The Cap ID outputs are read out as a low level differential voltage signal with LVDS-like levels, but with internal terminations (approx. 400 ohms). These outputs are only intended to drive a short distance (approx. 10 pF max. load) and are not intended to be terminated externally.

2. **CAPIDB(1)**. Cap ID output MSB complement.

3. **OUTISET**. This pad gives external access to the bias circuit for the low level differential voltage output drivers (CAPIDs, EXPONENTs, and MANTISSAs). It is included mostly for test purposes and nominally should be left unconnected. A resistor can be connected from VDD to this pad to increase the output drive level. The nominal resistance which exists internally is 3.4K.

4,5,6. **AGND1,2,3**. Analog ground pins, any or all of which can be used to return the bypass capacitor (for **AVDD1**, **AVDD2**, and **NI_AVDD**) to the internal die pad (analog ground).

7,8. **AVDD1,2**. Analog power supply pins. Connect together to +5V supply. Bypass to one or all of **AGND1,2,3**.

9. **NI_AVDD**. Non-inverting input amplifier power supply pin. Connect to +5V together with **AVDD1,2** if using the non-inverting input. Otherwise, connect to ground (**AGND4** is closest and easiest) to disable.

10,11,12. **AGND4,5,6**. Analog ground pins, any or all of which can be used to return the **NI_CLAMP** bypass capacitor to the internal die pad (analog ground).\

13. **NI_CLAMP**. Non-inverting input amplifier bias voltage, which must be bypassed to ground with an external capacitor of 0.1 uF. The bypass cap can be connected to any or all of **AGND4,5,6** to return it to the internal die pad analog ground. The **NI_CLAMP** voltage is generated internally, but can be externally pulled in order to tweak the input impedance value if necessary. Place an external resistor to ground or VDD as required.

14. **NI_RSEL**. Selects the input impedance of the non-inverting input amplifier. If unconnected, this pad defaults high (VDD), which sets the input impedance to 93 ohms. If grounded, the input impedance is 50 ohms.

15. **NI_ISET**. Non-inverting amplifier bias. Since the input impedance of the non-inverting amplifier is dependent on this bias value, no internal bias set resistor is present. A 1% tolerance external resistance should be used to set this bias value. Nominal is a 14K resistor to ground (300 uA).

16. **NI_INBIAS**. Non-inverting amplifier DC input bias current set. Set by connecting a resistor from this pad to VDD. The internal bias current will actually be 4 times smaller than the set value. Nominal set current is approximately 16 uA (4 uA amplifier

bias), which gives enough bandwidth to integrate a fast PMT pulse in one 25 ns bucket. This bias current can be adjusted to tailor the bandwidth. For nominal bias, use 220K.

17,19,21,23,25,27,29,32. **GND1,2,3,4,5,6,7,8**. Input signal ground pins. The ground planes which encase the signal traces should be connected directly to all of these pins.

18. **NI_INREF1**. Non-inverting amplifier reference input #1. This reference input ideally will have a cable or interconnect attached to it which looks identical to the signal input (although the reference input should actually have no signal applied to it).

20. **NI_INREF2**. Non-inverting amplifier reference input #2. An external resistor must be connected between reference input #1 and reference input #2. The value of this resistor depends on the desired input impedance. For 50 ohm input impedance, the R value should be 56 ohms, and for 93 ohm input impedance it should be 110 ohms.

22. **NI_INSIG1**. Non-inverting amplifier signal input #1. The signal input trace should be connected directly to this input, and should be completely encased with ground planes and traces right up to the pin.

24. **NI_INSIG2**. Non-inverting amplifier signal input #2. An external resistor must be connected between signal input #1 and signal input #2. The value of this resistor depends on the desired input impedance. For 50 ohm input impedance, the R value should be 56 ohms, and for 93 ohm input impedance it should be 110 ohms.

26. **I_INREF**. Inverting amplifier reference input. This reference input should have an interconnect attached to it which looks identical to the signal input (although the reference input should actually have no signal applied to it).

28. **I_INSIG**. Inverting amplifier signal input. The input trace should be completely encased with ground planes and traces right up to the pin.

30. **I_AVDD**. Inverting input amplifier power supply pin. Connect to +5V (tie to **AVDD1,2)** if using the inverting input. Bypass with 0.1 uF from the pin to the ground plane which is connected to **GND1-8**. If the inverting input is not used, connect **I_AVDD** to ground.

31. **I_INBIAS**. Inverting amplifier DC input bias current set. Set by connecting a resistor from this pad to ground. The internal bias current will actually be 4 times smaller than the set value. Nominal set current is approximately 4 uA (1 uA amplifier bias), giving a bandwidth appropriate for an input pulse which spans about 3 buckets (75 ns). The bias current can be adjusted to tailor the bandwidth. For nominal bias, use 750K.

33-36. **PED(0-3)**. Pedestal DAC inputs. Bits 0-2 control the pedestal magnitude (binary code, bit 0 is LSB) and bit 3 controls the polarity. Bit 3 low gives positive pedestals, and high gives negative pedestals. Each DAC bit gives approx. 0.6 ADC bits of pedestal,

therefore the pedestal range is from 0 to about 4 ADC bits, in each direction. If unconnected, the DAC pads all default low.

37. **DGBYP**. Digital ground bypass. This pin is for returning the DVDD bypass cap to internal die pad ground. It should NOT be externally grounded.

38,39. **DVDD1,2**. Digital supply connections (the two pins are redundant, only one is necessary). Connect to the same +5V supply as AVDD, but with a separate trace. Bypass locally as tightly as possible with a 0.1 uF capacitor from **DVDD** to **DGBYP**.

40. **RESET**. QIE reset signal. The reset signal should be approximately one clock period in duration. Each edge should occur near a positive going edge of the CLK signal. RESET is designed to accept a 3.3V CMOS level. A 5V CMOS level is also acceptable. After application of the reset, the capID is set to 0.

41. **CLK**. Clock input signal. CLK – CLKB accepts a low level differential signal (LVDS levels). QIE8 is designed for 40 MHz operation.

42. **CLKB**. Clock input complement.

43. **RANGE(0)**. Range 0,1 form a binary code which determines the range when the QIE8 is in fixed range mode (**FIX/AUTO** pin high). When in autorange mode (**FIX/AUTO** low), these bits have no effect, and the QIE8 automatically determines the appropriate range. Input levels are 3.3V CMOS. If unconnected, they default low.

44. **RANGE(1)**.

45. **FIX/AUTO**. Selects between fixed range mode (range determined by range 0,1 bits) and autorange mode. 3.3V CMOS level. Low selects autorange, high selects fixed range. If unconnected, defaults low.

46. **CALMODE**. Selects between normal mode and calibration mode. 3.3V CMOS level. Low selects normal mode, high selects calibration mode. Calibration is a high sensitivity (3X) limited span mode intended to be used only on the low range of the QIE8. (See table below). It allows a gain calibration to be performed by an input current source which has a magnitude of less than 1 LSB. If unconnected, **CALMODE** defaults low.

47,48. **DGND1,2**. Pins to the internal die pad ground which should be connected to the PC board digital ground plane. This should be the only connection point between the PCB digital ground and the QIE8 ground. The pins are redundant.

49. **MANT(0)**. Least significant mantissa (ADC) output bit. All outputs are low level differential voltage, as explained for pin 1.

50. **MANTB(0)**. **MANT(0)** complement.

51. **MANT(1)**.

52. **MANTB(1)**.

53. **MANT(2)**.

54. **MANTB(2)**.

55. **MANT(3)**.

56. **MANTB(3)**.

57. **MANT(4)**.

58. **MANTB(4)**.

59. **EXP(0)**. Least significant exponent (range) output bit.

60. **EXPB(0)**. **EXP(0)** complement.

61. **EXP(1)**.

62. **EXPB(1)**.

63. **CAPID(0)**.

64. **CAPIDB(0)**.

Following is a table which maps out the nominal charge sensitivity of the QIE8 over its 4 ranges. Note that each range is piece-wise linear, with the ADC assuming a "pseudo-logarithmic" response. In this way, the 5-bit ADC covers a 6-bit range, and tends to have a more constant resolution. The sensitivity at the bottom of a range is 5 times that at the top. Since adjacent range sensitivities differ by a factor of 5, the sensitivity at the top of a given range is the same as at the bottom of the next range. The calibration mode, intended to be used at the bottom of Range 0 only, offers 3 times higher sensitivity with limited range and linear response only.

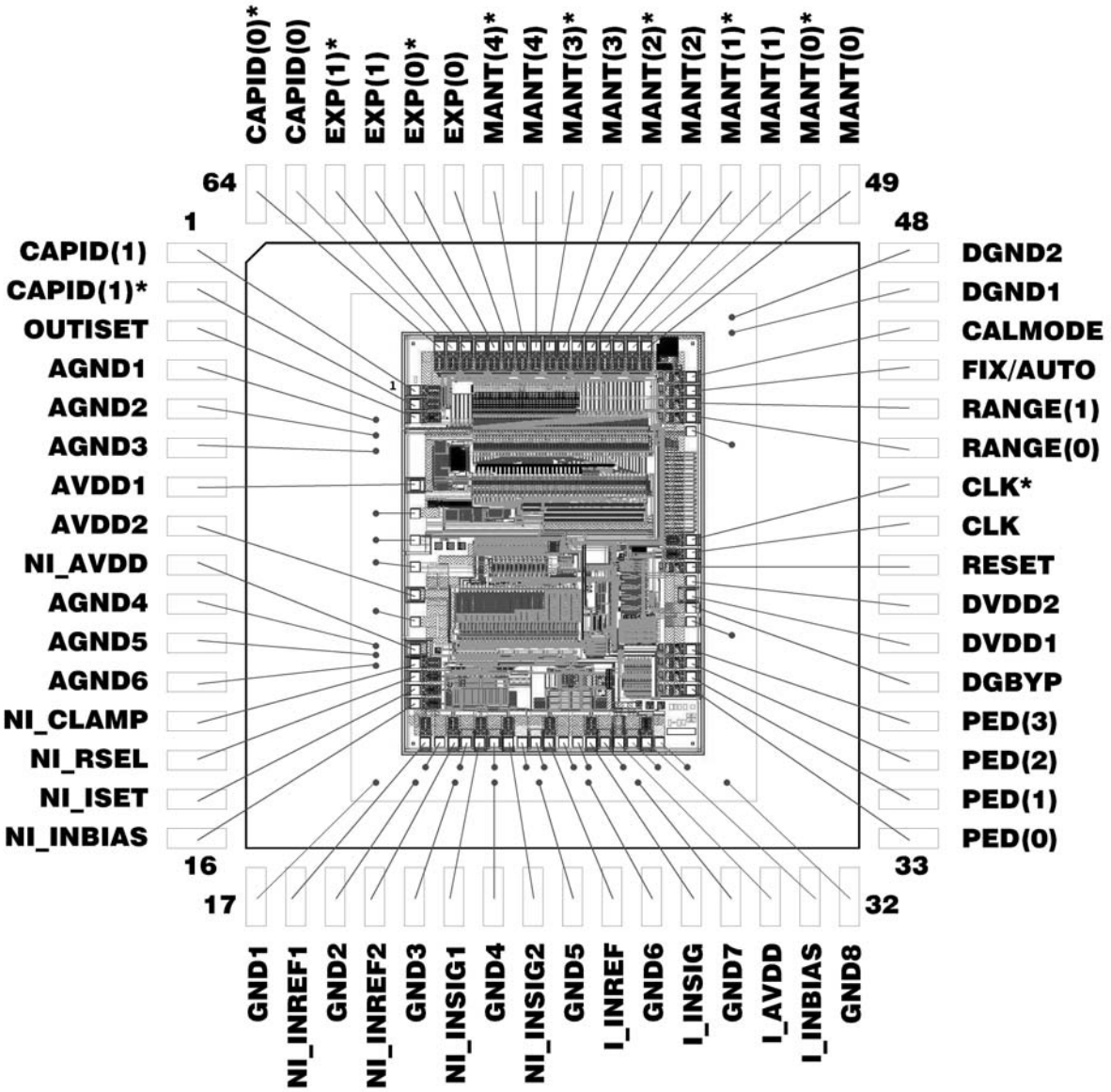
(Normal Mode)			
Range (Exp)	Input Charge	ADC Code (Mant.)	Sensitivity (Q/bin)
0	-1 fC – 14 fC	0 – 14	1 fC/bin
0	14 fC – 28 fC	15 – 21	2 fC/bin
0	28 fC – 40 fC	22 – 25	3 fC/bin
0	40 fC – 52 fC	26 – 28	4 fC/bin
0	52 fC – 67 fC	29 – 31	5 fC/bin
1	57 fC – 132 fC	0 – 14	5 fC/bin
1	132 fC – 202 fC	15 – 21	10 fC/bin
1	202 fC – 262 fC	22 – 25	15 fC/bin
1	262 fC – 322 fC	26 – 28	20 fC/bin
1	322 fC – 397 fC	29 – 31	25 fC/bin
2	347 fC – 722 fC	0 – 14	25 fC/bin
2	722 fC – 1072 fC	15 – 21	50 fC/bin
2	1072 fC – 1372 fC	22 – 25	75 fC/bin
2	1372 fC – 1672 fC	26 – 28	100 fC/bin
2	1672 fC – 2047 fC	29 – 31	125 fC/bin
3	1797 fC – 3672 fC	0 – 14	125 fC/bin
3	3672 fC – 5422 fC	15 – 21	250 fC/bin
3	5422 fC – 6922 fC	22 – 25	375 fC/bin
3	6922 fC – 8422 fC	26 – 28	500 fC/bin
3	8422 fC – 10297 fC	29 – 31	625 fC/bin
(Calibration Mode)			
Forced to 0	-2.33 fC – 10 fC	0 – 31	1/3 fC/bin

07/18/02

QIE 8 Production Pinout

64-Lead TQFP Package Bonding Diagram

(Drawing NOT to Scale)



QIE 8 Die Size: 3.070mm x 4.350mm
Die bond pad opening: 85 micron x 85 micron
Die bond pad pitch: 140 micron
Die bond pad metalization: Al (1%Si, 1%Cu)
Die Attach: Thermally Conductive

Notes: Package Pins 4, 5, 6, 10, 11, 12, 17, 19, 21, 23, 25, 27, 29, 32, and 47, 48 are bonded to the die attach pad.